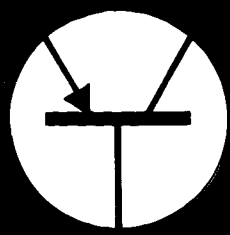

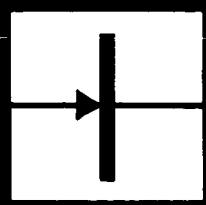

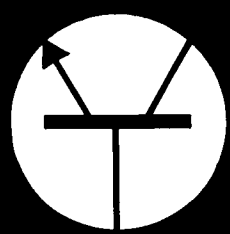

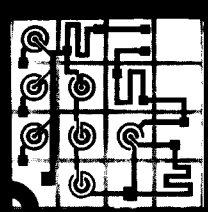

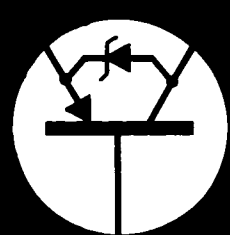

SEMICONDUCTOR PRODUCTS

Bendix Semiconductor Division
HOLMDEL, NEW JERSEY

THE Bendix CORPORATION

FIRST QUARTERLY PROGRESS REPORT

describing

DESIGN AND DEVELOPMENT OF A TEN NANOSECOND SEMICONDUCTOR SWITCH

Prepared by R. Reber, Design Engineer

C. Carroll, Project Manager

Approved by H. Newman, Chief Engineer

IN ACCORDANCE WITH CONTRACT NAS8-11611

FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER

NASA

HUNTSVILLE, ALABAMA

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PURPOSE OF CONTRACT

The purpose of this contract is to design, develop, fabricate and delivery five (5) prototype semiconductor switches and fifty (50) production units capable of meeting the end-result criteria outlined in Paragraph C-Design Goals of Contract NAS 8-11611. These design goals are restated in Section II.A of this report

I. INTRODUCTION

I. INTRODUCTION

The scope of work of this contract involves the design, development, fabrication and delivery of five prototype and fifty production semiconductor switches capable of extending the speed of high level switching transistors into the low nanosecond range.

Although a device of this type is not commercially available, the Bendix Semiconductor Division has recently developed a similar transistor which demonstrates that the design goals of the contract device are not beyond the state of the art.

Completion of this contract is to be accomplished in three phases, as follows:

Phas I - consists of the essential study and the preparation of a complete design of the units. Upon approval by the Contracting Officer such design will be employed for the prototype units under Phase II.

Phase II - consists of the fabrication of five prototype units and submission thereof to the Government for evaluation.

Phase III - consists of the fabrication of fifty production models modified in conformity with the changes, if any, required by the Government as a result of evaluation of the prototypes furnished under Phase II.

In its proposal, the Bendix Semiconductor Division scheduled completion of the contract within a nine month period. In accordance with this schedule, Phase I has been completed in all major details within the period covered by this first quarterly report.

The principal areas of Phase I which are discussed in this report include:

1) Determination of epitaxial starting material specifications,

2) Design of surface geometry,

3) Determination of concentrations and depths of diffused regions, and

4) Package design

A section devoted to the pertinent details of the major processing operations is included. Work to be performed during the next quarter (Phase II) is, also, discussed.

II. DEVICE DESIGN

II. DEVICE DESIGN

A. Design Goals: Criteria applicable to the semiconductor switches contemplated herein are as follows:

1. Mechanical Specifications:

   a. Hermetically sealed.

   b. Materials: Silicon Semiconductor crystal.

   c. Stud-mounting with double-ended case.

2. Environmental Specifications:

   a. Temperature Cycling: Minus 65°C to plus 200°C 5 cycles.

   b. Moisture Resistance: 10 cycles.

   c. Centrifugal: 1,000 g.

   d. Storage Life: Plus 200°C, 1000 hours.

   e. Shock: 500 g.

   f. Vibration: 20 g, 100 cps to 2000 cps.

3. Electrical Specifications:

   a. Collector-Emitter Breakdown Voltage BV_{ceo} (SUS) = 50 volts min.

   b. Collector cutoff current V_{ce} = 50v T_j = 20°C

      Collector cutoff current V_{ce} = 50v T_j = 200°C

   c. Emitter Cutoff current V_{eb} = 7 v T_j = 200°C

      I_{ebo} = 1 ma max I_c = 0

   d. DC current gain I_c = 10A V_{ce} = 4V, h_{fe} = 10 min.

   e. Saturation Resistance

      r_{ce} (sat) = 0.1 ohms max

   f. Base to emitter voltage I_c = 10A V_{ce} - 4v

      V_{be} (sat) = 2.0 v max I_b = 1A

   g. Turn on Time ($T_D + T_R$) I_c = 10A I_b = 1A

      T_{on} = 5 n sec max

   h. Turn off time ($T_S + T_F$)

      T_{off} = 5 n sec max V_{be} = -5v
      (assuming unsaturated condition) V_{cc} = 50v

4. Thermal Characteristics:

a. Collector Power Dissipation Tc - 25°C

Pc = 100 watts

b. Thermal Resistance

θj-c°C/watt, max. = 1.75°C/w

c. Junction Temperature Range

-65°C to 200°C

B. Epitaxial Starting Material

Starting material for the 10 ampere, 10 nanosecond switching transistor has been determined. The starting material comprises the very critical collector region of the device and consists of an "N" type epitaxial layer on an "N+" substrate. Detailed consideration has been given to both the structure (i.e. layer resistivities and thicknesses) and the overall quality of the material.

The basic decision to employ a double-diffused epitaxial collector design rather than a triple diffused structure has been made for two reasons. First, and most important, the epitaxial collector affords the best compromise among the device parameter of collector breakdown, capacitance and series resistance. Secondly, Bendix has had favorable experience with epitaxial starting material in construction of the "BIG Leaf" and other planar devices.

To optimize quality of the starting material, wafers have been ordered from three separate vendors. Specifications on the epitaxial layer thickness and resistivity have been made considerably tighter than those normally employed for Bendix planar power devices to insure that premium quality material is obtained. A preliminary evaluation of material supplied by the separate vendors is reported in Section IIIA.

Because of the predominant role of collector design on the device, parameters of (1) collector-base breakdown, (2) collector saturation voltage, and (3) collector-base junction capacitance, it is necessary to take all three parameters into consideration when

selecting the epitaxial layer resistivity and thickness. Parameters (1) and (3) improve with increasing resistivity and thickness while (2) is degraded. A compromise must, therefore, be made. For the purpose of this design the minimum resistivity and thickness required to meet the collector-emitter voltage specifications will be employed. This approach minimizes the collector series resistance. The collector junction capacitance will also be kept low, by employing an optimum collector junction area rather than by increasing collector resistivity beyond the voltage requirement.

The relationship between BVCBO, BVCEO and Beta can be approximated by

$$BVCBO = \beta^{1/n} BVCEO$$

where n is an empirical factor for "N" type silicon. From experimental data accumulated on Bendix planar devices, n ranges from 4 to 5. Based on these values of n and a Beta of about 30, BVCBO for this device must be a minimum of 100 to 120 volts. The collector body resistivity required to achieve avalanche breakdown voltages of this magnitude is approximately 2 to 3.5 Ω cm.

Minimum thickness for the epitaxial layer was calculated on the following basis:

(a) An out diffusion from the N^+ substrate into the N layer of 0.1 mil during processing.

(b) A base diffusion final depth of 0.2 mil.

(c) A condition such that most of the depletion takes place in the "N" region according to $Xm = \sqrt{\frac{2 K\varepsilon_0 V}{Q N_d}}$

A tabulated summary of the calculations involving layer resistivity and thickness is given below:

Collector Resistivity	BVCBO	BETA	n-4	n-5	Collector Thickness
2.2 Ωcm	103V	32	45 V	51 V	0.7 Mil
2.75 Ωcm	112V	32	49 V	56 V	0.77 Mil
3.3 Ωcm	120V	32	53 V	60 V	0.85 Mil

The design specification for the silicon substrate and the epitaxial layer is as follows:

Substrate

a.) Resistivity - .005 to .02 Ω cm.
b.) Doping - Antimony
c.) Orientation - (1-1-1)
d.) Thickness - $9 \pm .5$ mils
e.) Diameter - $1 \pm 1/16$"
f.) Lattice Structure - no slip, twins, or lineage
g.) Dislocation etch pits - as low as possible ($2000/cm^2$)

Layer

a.) Resistivity - 3.0 Ω cm ± 20%
b.) Thickness - .85 mil ± 15%
c.) Doping - Phosperous
d.) Edge Lip - None preferred (.25 mil accepted)
e.) Dislocations - $\leq 3000/cm^2$
f.) Stacking faults - $\leq 150/cm^2$
g.) Tripyramids & Prismatics - $\leq 10/cm^2$

C. Surface Geometry

The interdigitated structure shown in Figure I was selected because of its inherent high emitter periphery to emitter area ratio and because Bendix had past experience in fabricating interdigetated structures such as the Bendix "BIG Leaf". The overall dimensions were based on calculations and results obtained with the "Big Leaf" geometry. In particular it was our objective to significantly increase the emitter periphery in a geometry of the same or less surface area. This general plan of attack would enhance the B linearity, V_{CE} sat, f (t), and power handling capabilities of the device.

To achieve this basic goal several areas of the device construction were attacked and improved upon. These are:

1. optimize length, width, and taper of finger design
2. tighten spacing throughout design
3. minimize area of contact pads

To increase finger length while reducing the width it was necessary to increase aluminum contact thickness (see Section III D) and add a P+ base contact region (see Section III C), thereby maintaining negligible voltage drops along the fingers. This called for improvements or additions in diffusion, evaporation, and photo resist technology.

The reduced spacing demanded improved resist techniques i.e. masking, resist, alignment, and etching.

The reduced contact pad areas necessitated a new look at contacting procedures and philosophy. To minimize the possibility of device degradation and loss in yield it was decided that contact pads and/or fingers over the oxide would not be used. The base contact problem was solved by using two smaller leads (2 to 3 mil) at appropriate portions of the base geometry. The total base contacting area was therefore reduced to approximately 50 $mils^2$.

The emitter contact on the other hand could not be solved in this manner because the multiple lead approach would result in a larger overall contact area and increased lead inductance. The estimated wire diameter of 10 mils would normally necessitate a minimum aluminum pad of 15 mils x 30 mils (ultrasonic bond) or an area of 450 mil^2. This would demand extremely precise wire and bonding alignment. It was decided to bond the wire over the oxide protected base fingers at the center of the device leaving only a 3 mil wide emitter pad to insure finger connection. The bond would run the length of the active emitter so that each finger would essentially be tied directly to the wire. The success of this technique will be determined by the aluminum thickness, the oxide quality, and the bonding process. The resulting aluminum pad is approximately 100 mil^2 , i.e., less than 1/4 the area previously considered barely adequate.

The conductivity to the ends of the base fingers was insured by the P+ diffusion. This design scheme also appears to minimize the inherent heating effects normally noted at the emitter base junction around the tip of the base fingers i.e. close to the emitter lead.

Generally all fingers and contact areas were tapered and rounded to eliminate hot spots and/or leakage paths. Equal spacing of all geometries at all points was another consideration.

The resulting design compare to the Bendix "BIG Leaf" geometry as follows:

	NASA	BIG LEAF
Base Area	2175 mil^2	2500 mil^2
Emitter Area	1000 mil^2	1000 mil^2
Emitter Periphery	1000+ mil	550 mil
Base Periphery	175 mil	200 mil
Chip Size	60 x 80	80 x 80

Other areas of design criterion include circular alignment keys on each device chip and a 5 mil wide scribing path free of oxide and aluminum.

D. DIFFUSED REGIONS

Base Region:

Several requirements had to be taken into consideration in determining the concentration levels and depth of the base region. The BVEBO requirement of 7 volts limits the base surface concentration to a maximum value of approximately 7×10^{18} atoms/cc.

The BVCBO requirement imposes limitations on the base width - impurity gradient relationship. Working within these limitations, the base region has been designed to yield a high gain, high f_t structure. Thus, the device will employ the minimum base width and steepest doping gradient compatible with the aforementioned BVCBO and BVEBO requirements. Base surface concentration and base depth of 7×10^{18} atoms/cc and 4 μ respectively, will be employed for the prototype units. A base width of 1.0 μ is the design center.

Emitter Region:

Conditions for the emitter diffusion have essentially been determined by the base design criteria. The depth of this diffusion must be 3 μ to meet the requirement of a 1 μ base width. Concentration must be quite high ($\sim 10^{21}$ atoms/cc) to achieve the necessary injection efficiency into the highly doped base region required for high gain.

Simultaneously with the emitter diffusion an N^+ band will be diffused into the surface of the epitaxial collector layer in an area adjacent to and completely surrounding the base diffused junction. This band has two functions. It will serve to prevent channelling across the surface of the device from the base junction to the edge of the die. Secondly, it has been observed that such a band improves the gettering effects normally observed during phosphorous diffusion by virtue of its proximity to the collector-base junction.

P^+ Diffusion:

The primary purpose of this additional diffusion step has been discussed in detail under surface geometry design. There are two positive aspects of design for this diffusion. The primary requirement is to achieve a highly doped conducting layer within the base diffused region in order to optimize the device parameters of r_b', V_{BE} (sat), V_{CE} (sat) and B linearity. Another important function of the P^+ layer is to provide protection against the occurrence of a surface inversion layer over the more lightly doped base region.
From a negative viewpoint this region must be very carefully defined with respect to both lateral dimensions and penetration. The width of the P^+ fingers must be maintained accurately over their entire length and carefully aligned to prevent contact with the emitter diffusion. Such contact would lower the BVEBO of the device. With respect to penetration, the P^+ diffusion must be shallower than the base diffusion to insure that the BV_{CEO} is not influenced.

E. Package Design

Design of the package has been completed. The outstanding features of the design are:

1.) a 7/8" double-ended stud design capable of sustaining the 100 watts power dissipation of the transistor;

2.) a B_EO platform brased to the stud assembly to provide electrical isolation of all terminals from the package and thus minimise the effect of package capacitance on device switching characteristics; and

3.) a B_EO platform design which provides heavily metallised bonding pads for both emitter and base leads.

The purpose of this latter feature is to provide for a minimum length of bonding wire and to afford direct access to the bonding areas for ease of fabrication. The essentials of this package design are illustrated in Figure II.

III. FABRICATION PROCESS

III. A. Starting Material

Material was received from three vendors and evaluated by Bendix. A chart of wafer parameters in order of their importance has been compiled. Values in this chart may be referred to the specification values.

PARAMETER/SPEC	TEXAS INSTRUMENT	MONSANTO	GENERAL MICRO ELECTRONICS
Resistivity			
2.25 to 3.25 Ωcm	2.8 Ωcm	3.05 Ωcm	3.25 Ωcm
BV_{CBO} 100-125V	90-115V	110-145V	90-120V
Thickness			
.6 - .8 mils	.6 - .9 mils	.6 - 1.5 mils	.6 - 1.1 mils
Tripyramids & Prismatics			
$\leq 10/cm^2$	$\leq 10/cm^2$	$\sim 10\text{-}50/cm^2$	$100\text{-}250/cm^2$
Stacking faults			
$\leq 150/cm^2$	$10/cm^2$	$600/cm^2$	$2000/cm^2$
Edge Lip			
None preferred			
(.25 mil accept)	.6 - .8 mils	None	None
Dislocations			
$\leq 3000/cm^2$	$4000/cm^2$	$3000/cm^2$	$900/cm^2$

In general it could be said that the material received represented the vendor's capabilities and was consistent with results compiled on similar material for the BIG Leaf. The resistivity and thickness control normally exhibited by Texas Instrument as well as the superior surface topography qualifies them as the prime source for material for this device.

Although each specification is made by at least one of the vendors, no single vendor qualifies in all areas. The vendors have been contacted and made aware of the results of these tests with the hope that improvements will be forthcoming.

Devices which have been made from each of the vendor's material have been acceptable; however, differences in yield, distribution, and parameters do exist consistent with the control and surface topography of the respective vendors epitaxial material.

B. Surface Preparation

Prior to the initial thermal oxidation step, the epitaxial wafers are thoroughly cleaned. This operation consists of the following rather universal steps:

1. a TCE rinse to remove organic contaminants
2. an HF rinse to remove oxide films
3. chemical treatment to remove ion impurities and to provide a light protective oxide layer.

C. Diffusions

1. Silicon Dioxide Layers

The initial oxide layer is grown at 1050°C in a wet O_2 atmosphere. Thickness of this layer is 7000 to 8000 °A. During the base diffusion cycle an oxide layer of 5000 to 6000 °A is regrown over the base region to provide masking for this phosphorus diffusion. Following the emitter diffusion a thermal oxide of 2000 to 3000 °A is formed to mask against the subsequent P^+ diffusion. A final oxide layer of 2000 - 3000 °A is thermally grown after the P^+ step to provide masking during aluminum contacting.

Two problem areas exist with respect to the oxide layers. Because of the addition of the P^+ diffusion, the device sees three high temperature steps subsequent to phosphorus diffusion. Without the P^+ region the device would be processed through a single high temperature operation. Each of these three steps, namely, the P^+ deposition and the oxidations before and after P^+ effects both junction depth and impurity concentration at the surface. The transistor parametes effected are gain and BVEB. Consequently, the effects of these steps must be allowed for in the process or minimized.

To allow for these affects is possible but results in only a marginal degree of control and reproducibility. It appears more promising to minimize such effects. Proceeding along this line, investigations have been initiated to evaluate replacement of the thermally grown oxide layers with either pyrolytic oxides or a silicon monoxide evaporated layer.

The second problem area related to the oxide layer is its effectiveness as surface passivant. This area is discussed in a later section of this report.

2. Base and Emitter Areas

The base deposition step is performed in a B_2O_3 closed box system at 950°C. The diffusion is performed in a separate furnace at 1200°C. Times employed for the deposition and diffusion steps have been established to give a base surface concentration of between 5×10^{18} and 7×10^{18} atom/CC and a depth of 3.9 to 4.5μ.

The emitter diffusion is conducted at 1150°C using $POCl_3$ as the source. Time of the diffusion is determined by the evaluation of boron diffused control die from which the boron depth and concentration are measured.

3. P+ Diffusion

This step is carried out in a B_2O_3 closed system at 1100°C. It is a one-step operation so that the diffusion can be limited to a shallow surface layer. Some additional movement of this junction occurs during the final oxidation step.

D. Aluminum Evaporation:

The objective in Aluminum Evaporation has been a thick ($\geq$25,000Å), high quality aluminum film. It has been established that various evaporation procedures will directly effect the (1) etching rate, (2) edge definition and (3) etch factor (undercutting).

To date the best results have been achieved with the following conditions:

a) using parallel and individually controlled filaments

b) maintaining substrate at room temperature

c) maintaining vacuum in 3×10^{-6} torr range

A Bendix-Balzers vacuum system is being employed for this work.

Thickness measurements have been made using a sodium light and the interference objective on a Bausch & Lomb metallurgical microscope and confirmed with a Zeiss interferometer.

Evaporated aluminum purity and porosity have been the major difficulties. The use of an electron gun source and upward evaporation is being investigated.

E. Photo Resist

1. Masks:

With the completion of the geometry design a complete specification was written to tie down the dimensional tolerances and geometry quality acceptance criterion. Mask imperfections such as flaws, pinholes, spots, and peripheral defects are clearly defined by the specification, "Mask Acceptance" IN-156.

A thorough vendor evaluation was conducted with the emphasis on capability in mask construction and mask inspection. On the basis of this vendor evaluation and the quotes received, the decision was made to contract with the Qualitron Corp., Danbury, Conn.

The first shipment of masks received was inspected by Bendix and conditionally accepted to construct devices for initial evaluation. The masks failed to meet the spot and peripheral defect specifications and some of the dimensions were questionable.

During the past month a meeting between Bendix inspection people and the vendors Q.C. people resulted in dimensional correlation and an effort on the vendor's part to reduce spotting and peripheral defects.

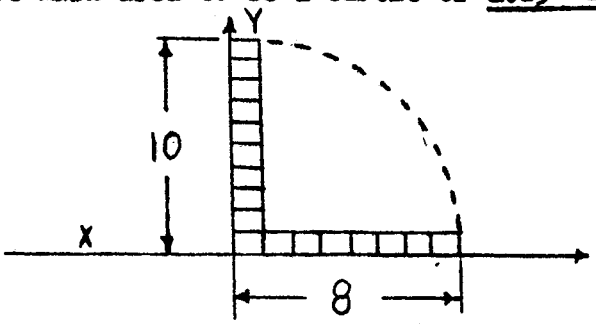
To reduce spots and scratches the vendor is re-evaluating his handling and packaging of masks. He believes that most of the problems occur in these areas rather than the quality of the plates as received from Kodak and inspected internally. In particular, the protective tape is suspected of leaving spots on the emulsion by trapping dust and dirt underneath. Perhaps the method of tape application is also causing flaws.

THE BENDIX CORPORATION BENDIX SEMICONDUCTOR DIVISION HOLMDEL, N. J.	**PROCESS SPECIFICATION**	Number - IN - 156
	MASK ACCEPTANCE	Pg. (1) of (2) Pgs.

A. GENERAL NOTES:

1. All dimensions ± .05 mil (50 millionths of an inch) exception noted

2. The active mask area to be a circle of 1.25" dia.



X dir ± 8 (.080") patterns
Y dir ± 10 (.060") patterns

3. The inspection area referred to in the specification to a circle of 1" dia. All patterns which fall within (better than 1/2 of the pattern is considered within) this circumference are covered by the following inspection criterion:

$\frac{1000}{80} \approx 12$ Xdir ± 6 Patterns inspected

$\frac{1000}{60} \approx 16$ Ydir ± 8 Patterns inspected

Approximately $150\ ^{+10}_{-0}$ patterns will be in the inspection area.

4. The cumulative tolerance of the total array of 12 patterns in the X direction and 16 patterns in the Y direction shall not exceed ± .050 mils. Registration (true position) from mask to mask to be within ±.100 mils.

5. Asterisks (*) Radius dimensions and centers are nominal however the parallelism of the registered patterns must be maintained, i.e. spacing between registered patterns ± .100 mils.

6. Breaks in the periphery of a pattern either into or out of the pattern are allowed if they protrude no further than the specification allows, i.e. .0001". However sharp spikes will be considered as grounds for rejection.

7. Grid work not critical - Dimensional accuracy ± .0002. No spec on breaks and/or pin holes.

8. True position of alignment dot centers to device centers must be ±.050 mils, dimensional tolerance of dot ± .0001".

9. The allowable number of defective patterns within the 1" dia. inspection circle (≈ 150 patterns) not to exceed (7) seven ≈ 5%.

(cont'd page 2)

APPROVALS: R. REBER DATE: 5-8-64

Prepared by:	R.L Reber	5-13-64
Product Manager:		5-14-64
Industrial Engineer:		5-14-64
Q.C. Manager:		5/18/64
Authorized:		MAY 19 1964

ENGINEERING CHANGE RECORD

ECO	DATE	CHECKED
3104	5-13-64	RLR
3104A	5-21-64	RLR

THIS SPEC. SHEET NOT RECORDED AND WILL NOT AUTOMATICALLY BE REPLACED WHEN CHANGES ARE MADE.

9. (continued) Defects defined as discrepancies in geometry and/or dimensions, spots and pin holes (see individual mask specifications), lines, scratches, etc.

10. The allowable number of defective glass plates shall not exceed 5% in any one shipment.

11. Border of glass tile to be opaque.

12. Mark tool # and Issue letter on all masks and original art work.

13. The glass plates to be cut 2" ± 1/16 sq. with pattern (grid lines) parallel to the cut edges and the active mask area centered to within ±0.1".

C. SPECIFIC SPECIFICATIONS:

1. Base Mask. Geometry rejection criterion.
   a. Pin holes in the opaque (base area) greater than 0.080 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils in the clear area within 0.001" of the base are not allowed.

2. P^+ Geometry rejection criterion.
   a. Pin holes in the opaque (P^+ area) which are greater than 0.20 mils dia. are not allowed.
   b. Opaque spots greater than 0.10 mils dia. in the clear area are not allowed. Clear area defined to be all clear area within 0.002" outside P^+ geometry.

3. Emitter. Geometry, rejection criterion
   a. Pin holes in the opaque (emitter area) greater than 0.080 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils dia. in the clear area are not allowed. Clear area defined to be all clear area within .0005" inside guard ring.
   c. Guard ring dimensional tolerance ± .0001". Pinhole spec does not apply to guard ring.

4. Contact Cut: Geometry rejection criterion
   a. Pinholes in opaque (Contact Cut Areas) greater than 0.20 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils dia. in the clear area are not allowed. Clear area defined to be all clear area within 0.0015" outside contact geometry.

5. Al Contact Cut. Geometry rejection criterion
   a. Pin holes in opaque (area to be etched) greater than 0.10 mils dia. not allowed. Opaque area defined to all opaque area within 0.0015" outside al contact geometry.
   b. Opaque spots greater than 0.20 mils dia. in the clear areas are not allowed.

The pattern edge irregularities were not seen on the master plates. The problem was traced to the reproduction process. Additional controls will be instituted to minimize these processing irregularities. When these areas of investigation and control are completed a shipment of masks will be ordered and fully evaluated.

2. Oxide & Aluminum Etch

The photo-chemical technique has been carefully scrutinized to establish weak or marginal processes. The present system using Kodak KPR-KPL at high spinning speeds appears to offer advantages in etch resistance, adhesion, and definition. Micro-filtration of all chemicals and minimum handling of wafers in process has resulted in cleaner reproductions and should enhance yield. The Micro-mechanics alignment and exposure system has the alignment tolerance and exposure conditions deemed necessary. Development is accomplished in standard Kodak chemicals baths. Etching of the wafers is done in an ammonium fluoride - HF etch.

Coating and alignment (Exposure) operations are in absolute filter dust boxes while all other operations are in 0.5 micron dust boxes.

Photo-micrographs of the geometry reproductions were included in the third monthly report. Figures I and II.

Etching of thick aluminum layers with adequate definition was accomplished by using KTFR (Kodak Thin Film Resist and a Phosphoric-Nitric-H_2O etch. The additional adhesion and etch resistance of the KTFR ideally suited it for this operation. The etching rate of the Phosphoric-Nitric-H_2O solution is dependent upon temperature; which has made it possible to establish optimum conditions for etching of the aluminum contacts. (See Attached Photo.: Figure IV.)

Resist removal is accomplished in hot sulphuric acid solutions and/or in commercially available resist strippers.

F. Surface Passivation

The use of thermal oxides in planar processing can be improved thru densification and/or combination with prolytic technology. A good gauge of oxide quality is the number of pin holes/unit area. In order to test the various oxide techniques, a chlorine etch system has been designed and will be set-up shortly. Thusly, any flaw or imperfection in the oxide will permit etching of the silicon subsurface by gaseous chlorine.

The combination of wet and dry thermal oxides has proved quite successful. However, the pyrolytic oxide may be advantageously employed as the final device layer. The process is carried out a a lower temperature and therefore will minimize junction travel after device manufacture. The silicon dioxide layer formation also does not require silicon surface atoms but is provided totally by the thermal cracking of an organo silane compound.

Solutions have been developed by this laboratory which offer satisfactory removal of both boron and phosphorus glasses formed during diffusion. Prior to contact metallization, it may be worthwhile to replace all glassy structures with a fresh passivated layer. This process is under investigation to ensure stable device characteristics and optimize electrical performance.

G. Assembly

During the first quarter preliminary discussions on the package design were held with two potential vendors, National Beryllia and Electrical Industries. As a direct result of these discussions engineering sketch ES-116 of the proposed Beryllia isolation pad was laid out. This design provides for minimum lengths of bonding wires and ready access to the bonding areas for ease of fabrication. After final design details were resolved an initial sample order for evaluation of the package design was placed with National Beryllia Company. The design is shown in Figure II. First samples of the platform assembly have just been delivered and are in the process of being checked for conformity to the drawing.

During this same period a heat column for die mounting was designed (see Figure III) and ordered. Final assembly of this fixture is now in process. Four sizes of pure (99.99%) aluminum bonding wire, .007, .008, .009, and .010 dia and the necessary tungsten carbide bonding capillaries for each were ordered and delivered. Initial bonding experiments produced bonds which withstood an axial pull great enough to break the wire.

IV. CIRCUIT DESIGN & TEST RESULTS

IV. CIRCUIT DESIGN:

The optimization of the BIG Leaf characteristics for switching parameters was completed during the first phase of the program. Circuit design development of the 10 - Ampere switching circuit has progressed to the point where the optimum switching parameters of the BIG Leaf were obtained at the 5 - Ampere level. Separate turn-on and turn-off circuits were designed in order to obtain the best possible switching characteristics for each of these parameters. The finalized circuits for the BIG Leaf transistor appear in Figures V and VI. The experimental BIG Leaf devices were evaluated in the turn-on circuit of Figure V. The switching times in this circuit are summarized below.

t_d = 3nsec and t_r = 15 nsec

These turn-on times were obtained at a collector current of 4 Amperes, due to the limitation imposed on the collector supply voltage by the breakdown of the experimental devices. Diodes D_1 and D_2 prevent the collector-base junction from entering the saturation region. The response of D_2 affects the measurement slightly, and faster diodes will be utilized for this circuit in the second phase of the program. The turn-off times for these transistors were obtained in the circuit of Figure VI. Typical results are indicated below.

t_s = 4 nsec and t_f = 7nsec

These results were obtained when the transistors were switched from the 4 Ampere conducting condition to cutoff; provided by

the reverse bias of V_{BB} as indicated in Figure VI. Diodes D_1 and D_2 form a Baker clamp circuit, keeping the collector-base junction out of the saturation region. In this manner, the low storage times provided by a non-saturated circuit are utilised. The present diodes will have to be replaced by other types with a faster response time, since the diodes now in the circuit tend to slow the response of the turn-off wave form in the collector circuit. The pulse width for each of these test circuits was 100 μsec; and eventually will be reduced to 50 μsec, or less. The pulse width must be kept at least as large as the turn-on plus turn off times of the device-under-test for correct response-time measurements. All leads to external bias supplies have been by-passed with suitable capacitors to keep lead inductance in the circuits to a minimum. The current transformer, T_1, in each of the circuits is used to observe the current pulse applied to the base of the transistor. In this manner, the diode clamping action is seen; and proper base currents determined from this observation. At the present time, each transistor must be soldered into the test circuits for evaluation. An experimental test socket is being designed to eliminate this procedure. This socket will provide short lead lengths from the circuitry to the transistor pin connection, while providing shielding between input and output for proper isolation at the high switching speeds encountered in the testing of these devices. The successful utilization of this socket will enable the testing of both experimental and production devices to be conducted at a

more feasible rate than is now possible.

The second phase of the program will include the evaluation of the initial newly-designed power-switching transistors fabricated by Development Engineering. All pertinent characteristics will be measured, and progress in circuit design will proceed concurrently with device improvement. Initial switching measurements will include evaluation at an I_C = 5.0 Amperes in order to compare the power-switching device to the BIG Leaf.

V. PROGRAM FOR PHASE II

V. PROGRAM FOR PHASE II

A. Device Design

Whereas PHASE I concerned itself primarily with determination of the design details, PHASE II efforts will be, for the most part, in the areas of fabrication and evaluation of prototype devices. However, improvements or modifications to the preliminary design will continually be undertaken wherever it appears necessary or advantageous to do so. The extent of efforts in this area will be largely determined by the performance of prototype units with respect to the design goals.

B. Fabrication Processes

1. Starting Material

Effort will continue in this area toward more tightly defining epitaxial starting material quality. This will necessitate correlation of yield and performance data with specific material parameters.

2. Diffusions

Considerable effort will be expended in the area of oxide formation and diffusion. Investigation into the replacement or supplementation of the thermally grown oxides after phosphorus diffusion with low-temperature oxide techniques (such as pyrolytic oxide) will be made.

Firm process control specifications will be determined for base and emitter junction depths and layer concentrations.

P+ diffusion will be examined extensively. This will include evaluation of devices made with and without the P+ step. It will also involve performing the P+ diffusion at different places in the process.

3. Aluminum Evaporation

Additional work must be performed to improve the quality and reproducibility of the 25,000 A aluminum contact layer.

4. Photo Resist

The photo resist (KPR-KPL) system outlined in Section III. E appears to produce the desired results. Unless unforeseen problems become apparant or process innovations are necessary the KPR-KPL process will not be altered.

The KTFR process for etching of thick aluminum will be firmed up in the next month, however, initial results from this process indicate little or no improvement is necessary.

Of specific interest for this project is a new Kodak product KPR Type II. This product is on order and an evaluation of KPR II will be forthcoming. This resist should offer several advantages, namely:

1) New solvent system (not water miscible)

2) Higher viscosity (2x std. KPR)

3) Slightly higher solids content

4) More stable and cleaner

5. Assembly

Although fixtures and tooling were designed in this past phase for assembly of the prototype devices, no actual assembly operations have been performed to date. This is

simply a result of the fact that packages of the new design have just recently been received. Consequently, much effort will be spent in PHASE II toward establishment of the assembly steps of die mounting, wire bonding and doming.

Experience with other planar devices at Bendix has shown a definite relationship between device parameter and their stability and control of such assembly conditions as ambient, cleanliness and especially humidity. All assembly operations on the prototype devices will be accomplished in recently completed dry box line.

C. Circuit Design and Test Results

Evaluation of prototype devices and of various test circuits will constitute a major portion of PHASE II activity.

Data will be accumulated and analyzed on all pertinent electrical and thermal parameters of the prototype devices. Close laision with both design and fabrication areas will be maintained so that conclusions reached from device performance data can be immediately reflected in process modification and/or device design.

Switching speed characteristics will be of predominant interest. All finally assembled prototype units will be thoroughly examined in the switching test circuits regardless of whether or not other parameters are within specification.

Refinement of the switching circuits will continue. Specifically, evaluation of faster diodes in the switching circuit will be made; and the experimental test socket discussed in Section IV will be evaluated.

D. Environmental Specifications

In order to initiate environmental testing at the earliest possible date, prototype devices which have been completely evaluated electrically will be made immediately available. It must be understood that devices subjected to environmental testing during this phase will not necessarily be representative of the five prototype units submitted at the end of PHASE II.

E. Submission of Prototype Devices

Based on progress to date, it is estimated that the five necessary prototype devices required to terminate PHASE II will be submitted within the next quarterly period.

VI. KEY PERSONNEL

VI. Key Personnel

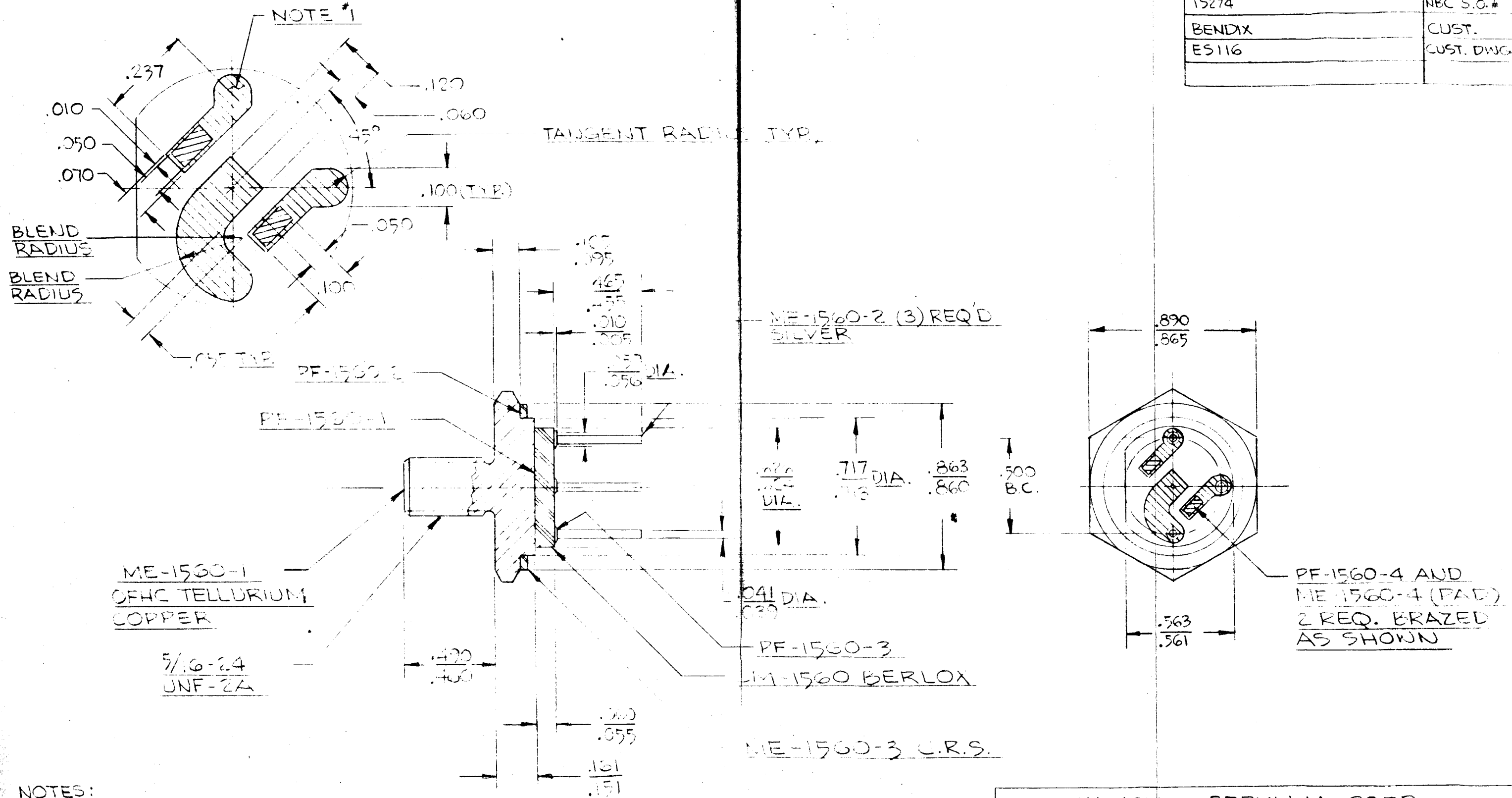
Mr. Charles Carroll has been named Project Manager of the subject program. Mr. Carroll replaces Mr. Albert Schrob. This personnel change was prompted by the fact that the preliminary design goals have been met and that the subsequent preproduction and final units will be manufactured in accordance with plans and specifications developed during the Phase I portion.

Mr. Carroll's experience as a development engineer, working in the area of silicon power transistors, coupled with his previous participation in this program, should further assure the successful completion of the devices to be furnished.

Mr. Schrob will continue to serve on an advisory basis and will be appraised of the progress of this contract until all work is completed.

A-1560

15274	NBC S.O.#
BENDIX	CUST.
ES116	CUST. DWG.



NOTES:

1-METALLIZED AREA .0002 GOLD MINIMUM.

2-FINISH ON STUD TO BE A MINIMUM OF .0001 GOLD.

NATIONAL BERYLLIA CORP.

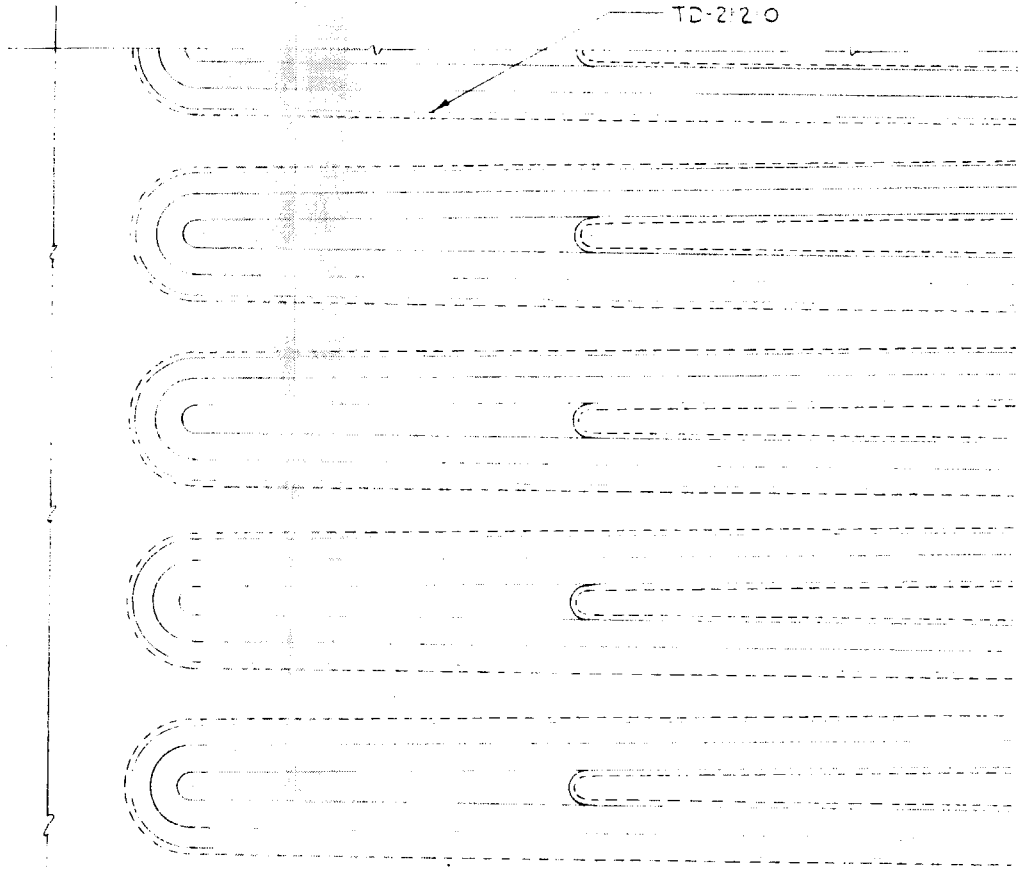
SCALE 2:1

7/8 HEX. NAIL HEAD ASS'Y OUTLINE

DRAWING NO. A-1560

ES-119

NOTE: 1. DO NOT SCALE DRAWING
2. REPORT ALL ERRORS



N

3

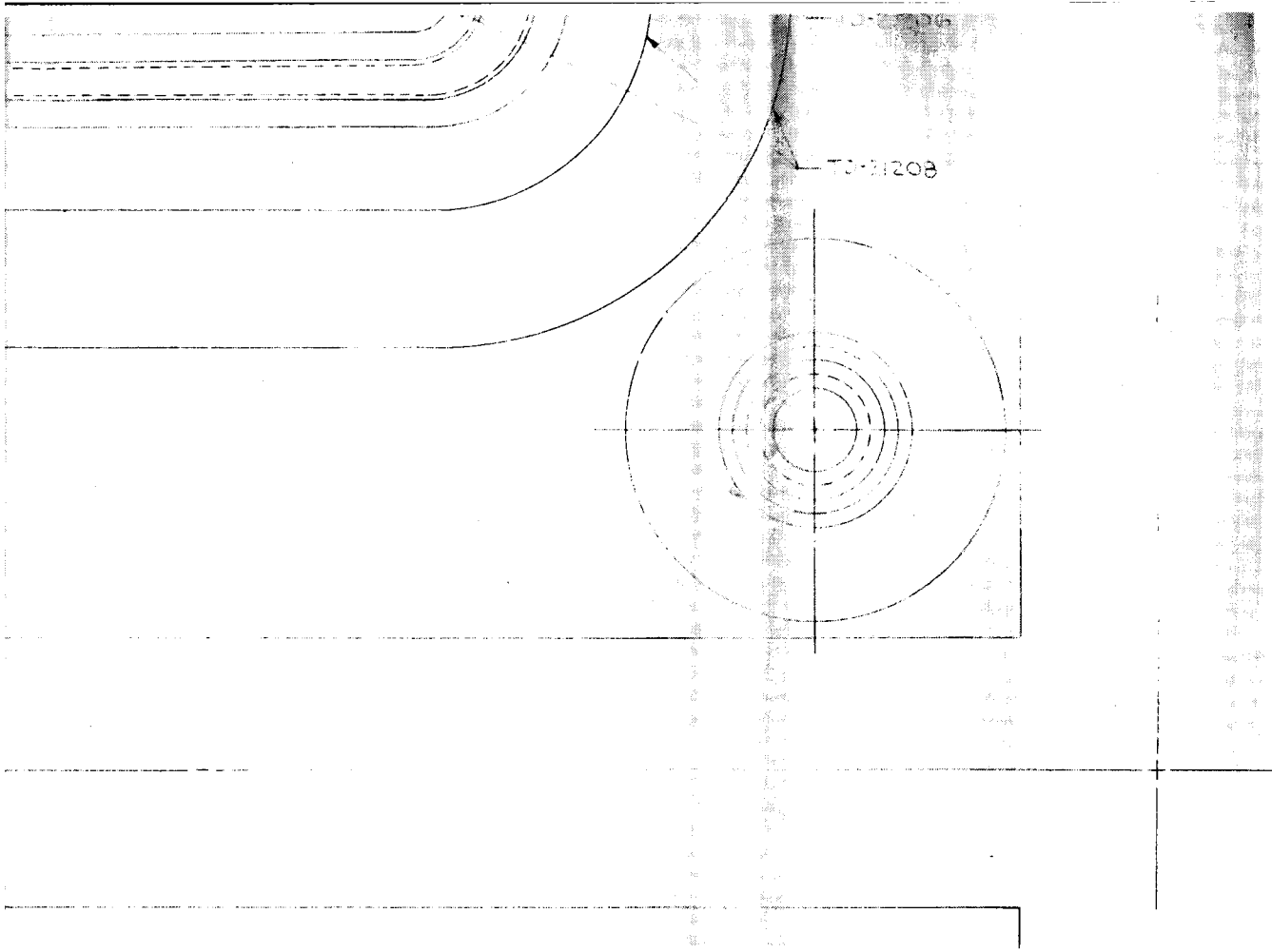
TOOL NO.	ISSUE
TD-21205	-A

REVISIONS

ISSUE LTR	DESCRIPTION	DATE	BY	CHK
A	ECO 3034	5-8-[illegible]	EM	[illegible]

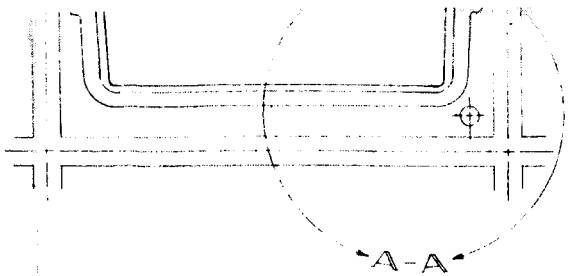
C

DETAIL A-A
SCALE 500/1



UNLESS OTHERWISE SPECIFIED

1. REMOVE ALL BURRS AND SHARP EDGES _____ MAX.
2. ALL CORNERS SHALL HAVE FILLETS OF _____ RAD (APPROX TRUE).
3. ~~TOLERANCES ON LINEAR DIMENSIONS (INCL HOLES):~~
   ~~2 PLACE DEC. ±.010; 3 PLACE DEC. ±.005; FRACTIONS ±.015;~~
   ~~ANGULAR ± ½°; EXCEPT ±.25 ON 45° CHAMFERS LESS THAN .040.~~
4. THREAD LENGTH DIMENSIONS ARE FOR FULL FORM THREADS.
5. ROUGHNESS NOT TO EXCEED THE FOLLOWING MICROINCH VALUES FOR: MACHINED SURFACES _____ ; SURFACES MARKED √_____ .
6. SYMBOLS ⊙, ⊥ AND ⌯ SHOW THAT SURFACES INDICATED BY ARROWS OR SOME LETTERS, E. G. (A), MUST BE HELD CONCENTRIC, SQUARE OR PARALLEL RESPECTIVELY WITHIN THE LIMITS SPECIFIED.



	1		ALUM. CONTACT MASK	TD-21210
	1		CONTACT CUT MASK	TD-21209
	1		EMITTER & GUARD MASK	TD-21208
	1		BASE P+ MASK	TD-21207
	1		BASE REGION MASK	TD-21206
ITEM	QUAN.	TOTAL QUAN.	MATERIAL	SIZE - ALLOW FOR FINISH

SCALE NOTED

DRAWN	E.M.	4-22-64
CHECKED		
M.E.		
ENG.		

PART REF. | TYPE REF.

FINISH

HARDNESS

THE Bendix CORPORATION
Red Bank Division
SEMICONDUCTOR PRODUCTS
HOLMDEL, NEW JERSEY

TITLE
POWER SWITCHING TRANSISTOR

TOOL NO. TD-21205-A ISSUE A

TOOL NO. TD-21205-A ISSUE A

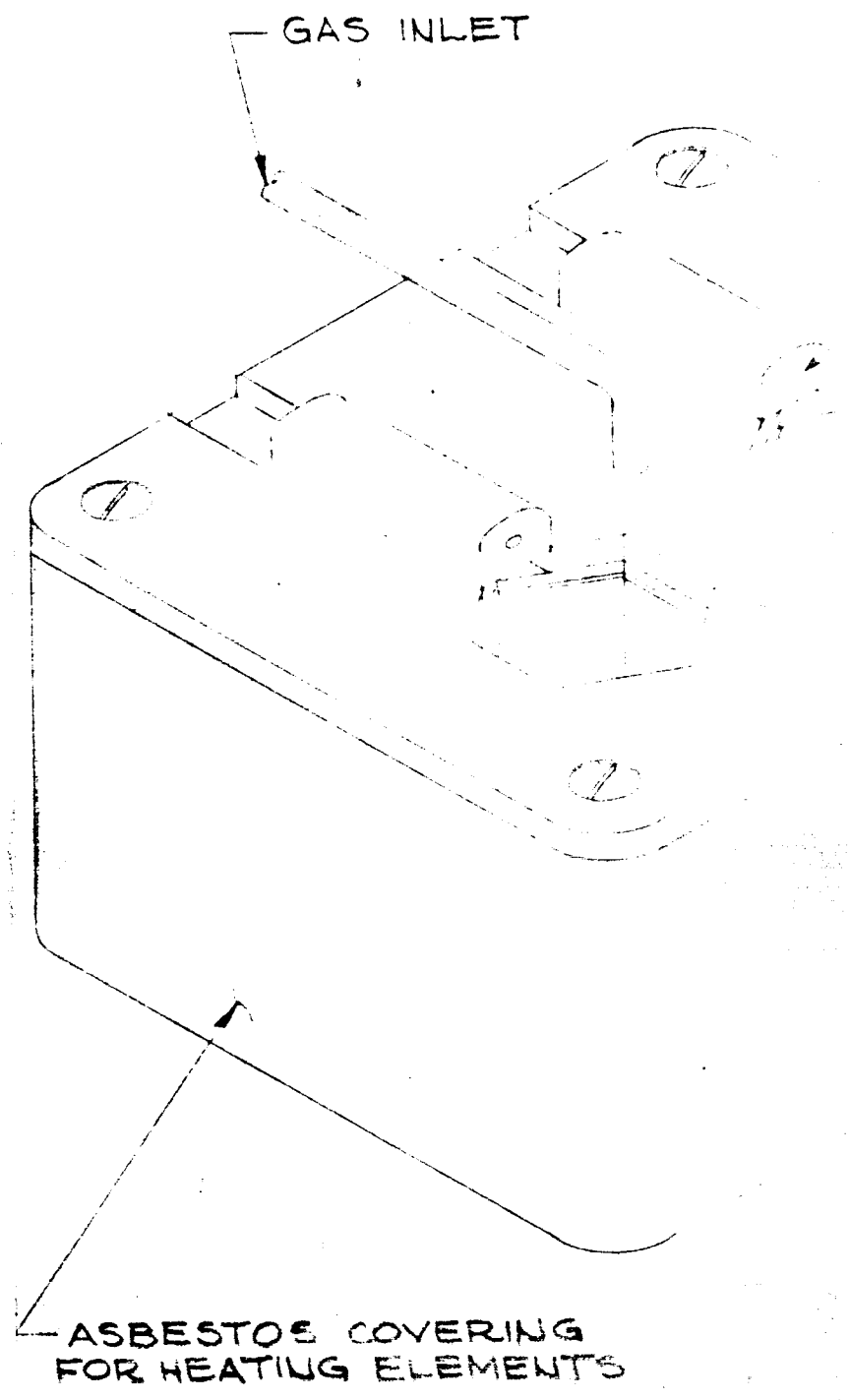
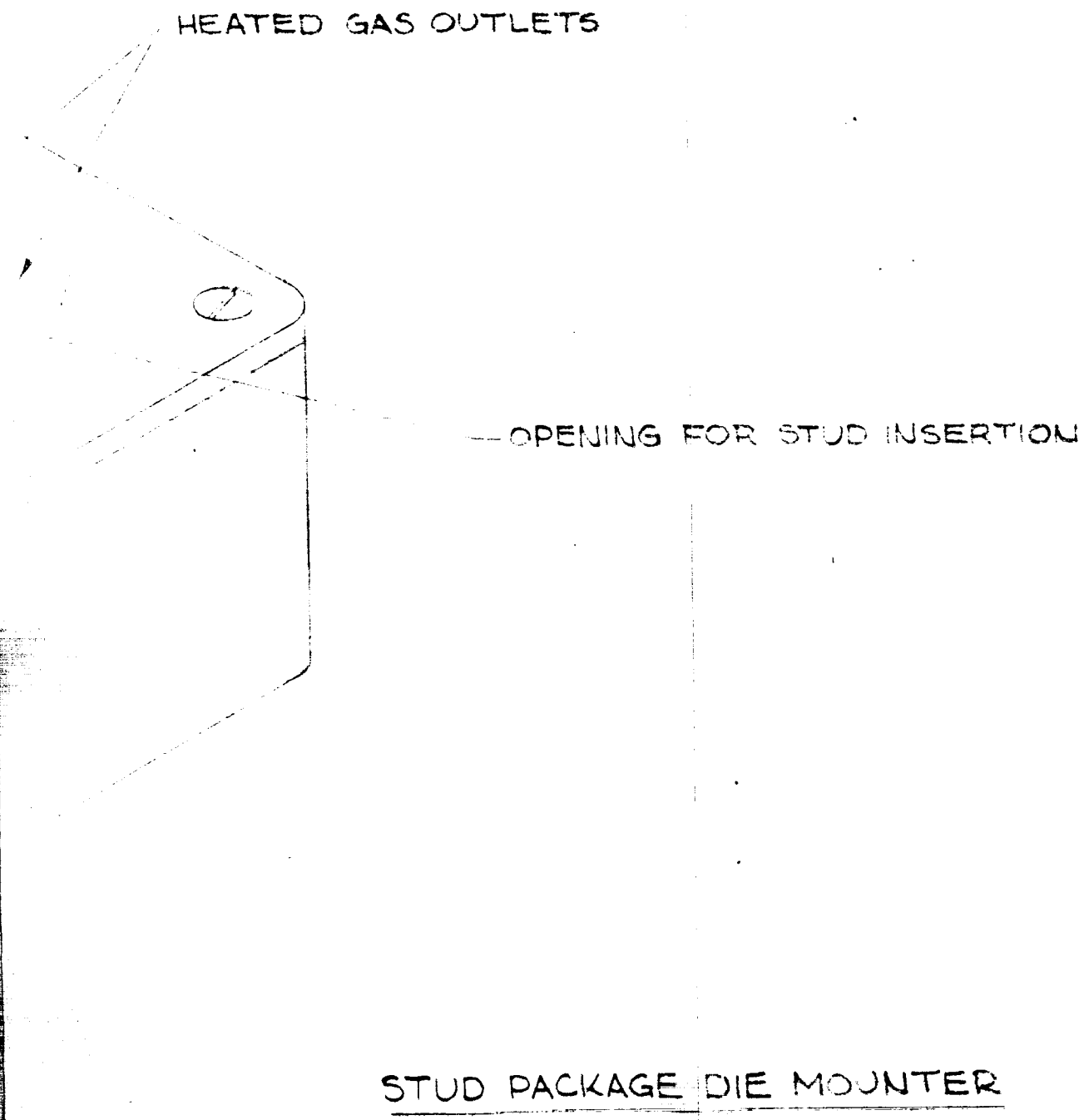
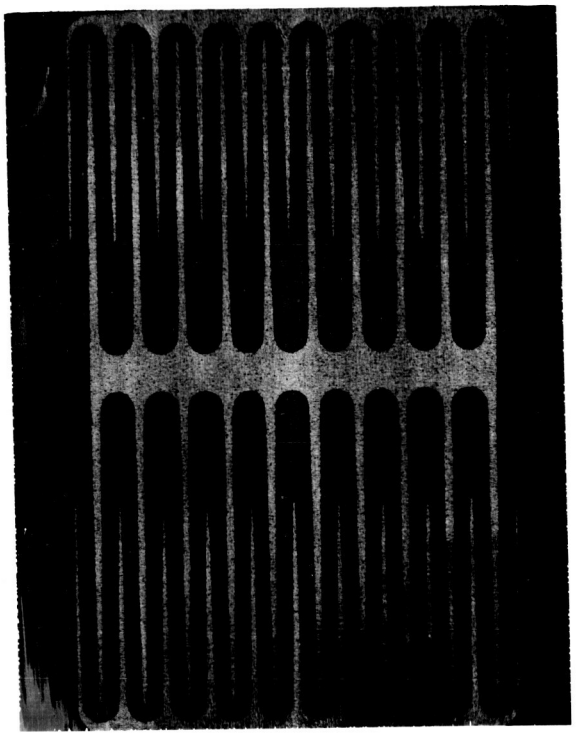


FIG. I



STUD PACKAGE DIE MOUNTER

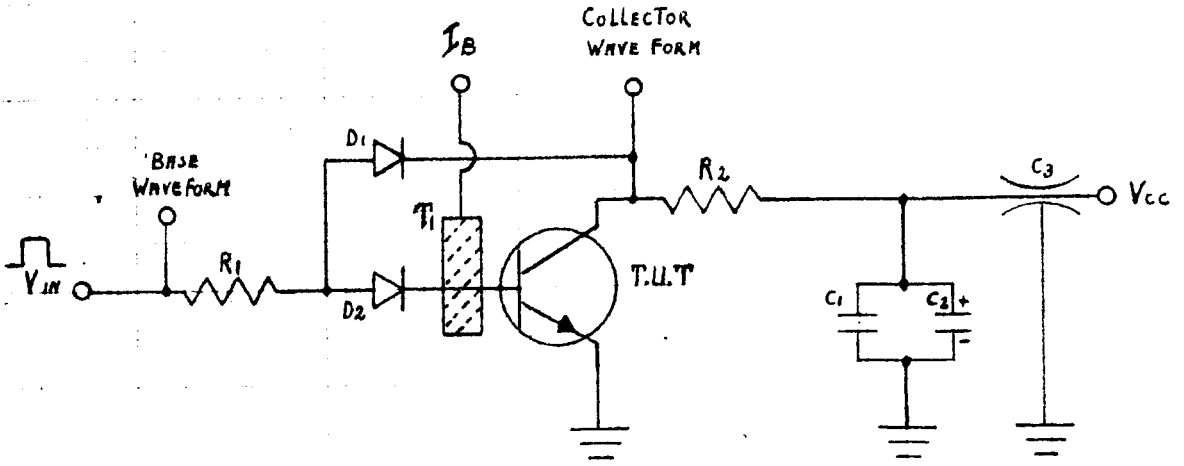
FIG. II



ETCHED ALUMINUM CONTACT PATTERN

(25,000Å)

FIGURE IV



C_1 - 0.3 mf 100 V
C_2 - 30 mf 150 V
C_3 - 1000 Pf FEED-THRU
D_1 - IN3600
D_2 - IN3606

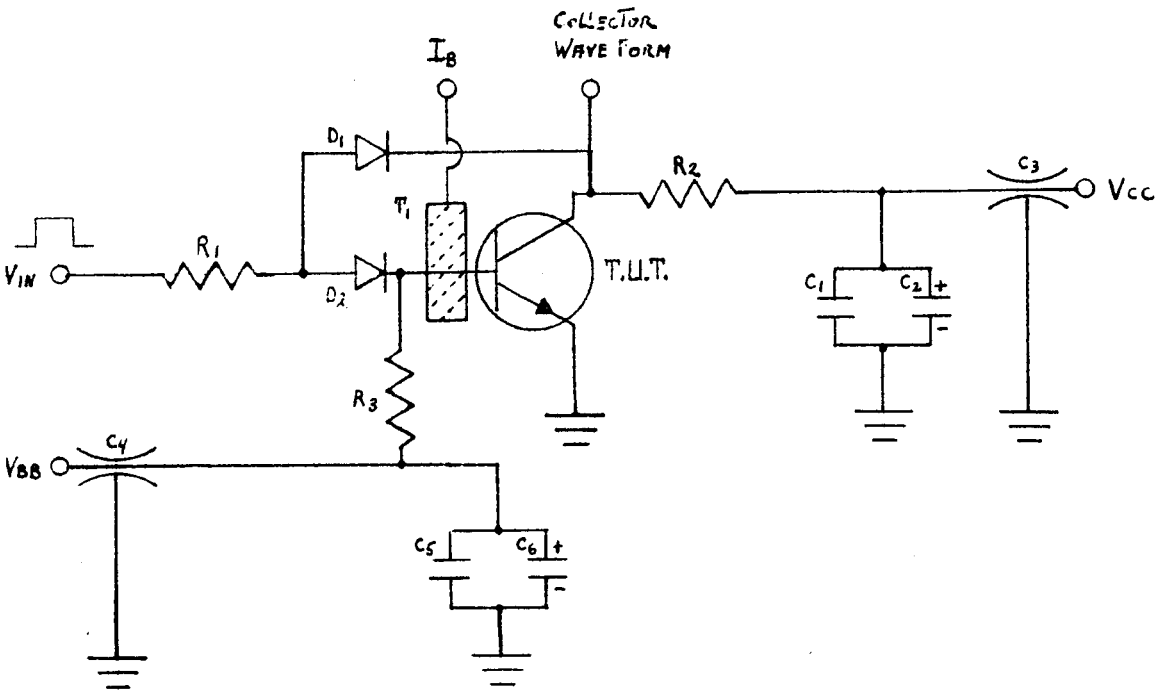
R_1 50 Ω 1W
R_2 5 Ω 1W
} METAL-OXIDE FILM

T_1 TEKTRONIX CURRENT TRANSFORMER CT-1

				CONDITIONS			
	t_d	t_r	t_{on}	V_{cc}	I_c	I_{Bon}	PULSE WIDTH
	nsec	nsec	nsec	V	A	A	nsec
1.	2	15	17	26	4	0.4	100
2.	3	16	19	26	4	0.4	100
3.	3	15	18	21	3	0.3	100

TURN-ON CIRCUIT

FIGURE -V-



C_1 - 0.3 μf 100V
C_2 30 μf 150V
C_3 - 1000 Pf FEED-THRU
C_4 - 1000 Pf FEED-THRU
C_5 - 0.3 μf 100V
C_6 - 30 μf 150V

D_1 - IN3600
D_2 - IN3606
R_1 - 50 ~ 1W
R_2 - 5 ~ 1W } METAL-OXIDE FILM
R_3 - 5 ~ 1W
T_1 - TEKTRONIX CURRENT TRANSFORMER CT-1

	t_s	t_f	t_{off}	V_{CC}	I_C	V_{BB}	$I_{B\,off}$	PULSE WIDTH
	nsec	nsec	nsec	V	A	V	A	nsec
1.	5	15	20	26	4	-5	-0.4	100
2.	4	7	11	26	4	-4	-0.3	100
3.	2	4	6	21	3	-3	-0.3	100

TURN OFF CIRCUIT

FIGURE -VI-